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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,776	09/22/2000	Takashi Yoshikawa	05225.0168	8165

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EXAMINER	
ROCHE, TRENTON J	
ART UNIT	**PAPER NUMBER**
2124	7

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

7

Office Action Summary	Application No.	Applicant(s)	
	09/667,776	YOSHIKAWA, TAKASHI	
	Examiner	Art Unit	
	Trent J Roche	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to Amendment A filed 08 March 2004.

2. Per applicant's request, amended claims 1-4, 11, 14 and 22-24 have been entered. Claims 1-24 are pending.

3. Claims 1-24 have been examined.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/667,776, filed on 09/22/2000.

Drawings

1. The drawings were received on 08 March 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 23 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 23 recites moving an instruction sequence speculatively executable forward an instruction sequence not speculatively executable in the program. It is stated on page 23 of the remarks that

amended claims 1 and 24 include similar recitations, and as such, both include the aspect of an instruction sequence speculatively executable being moved forward an instruction sequence not speculatively executable in the program. The applicant states that support for the amendment can be found on at least page 50 of the specification. Upon further examination, the Examiner has not found sufficient support for the amended material in the recited portion of the specification. While the cited paragraph of page 50 does disclose a data dependence sequence being moved forward, this sequence is *speculatively moved forward* (emphasis added), in other words, it would appear that once the data dependence sequence is determined to be a candidate for speculative processing, the sequence is moved forward *after* the processor speculatively executes the sequence. Accordingly, the cited passage does not appear to disclose a reasonable teaching for moving an instruction sequence which is determined to be a candidate for speculative processing forward an instruction sequence not speculatively executable in the program, but rather what occurs once a sequence has been speculatively executed by the processor. Furthermore, consistent with the claims as originally filed, the specification states in two instances the opposite of moving an instruction sequence speculatively executable forward an instruction sequence not speculatively executable. First, note page 24, which states "a non-speculative instruction is executed before a speculative instruction." Second, note page 60, which states "the compiler clearly indicates whether the instruction is speculative, and non-speculative instructions are executed before speculative instructions." These citations appear to be inconsistent with the aspect of moving an instruction sequence speculatively executable forward an instruction sequence not speculatively executable. As such, claims 1, 23 and 24 are rejected under 35 U.S.C. § 112, 1st paragraph.

For purposes of examination, as it is not clear how the claimed invention is intended to operate, the aspect of a non-speculative instruction being executed before a speculative instruction, as stated in originally filed claim #2 and the originally filed specification, will be considered as the relevant inventive concept and that the amendment intended to recite these limitations.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 2 recites the limitation "the instruction of data production or data consumption..." in lines 3-7. There is insufficient antecedent basis for this limitation in the claim.

For purposes of examination, this will be interpreted to read "the instruction sequence..."

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,511,172 to Kimura et al.

Regarding claim 1:

Kimura et al teach:

- a central processing apparatus for assigning instructions of a program to a plurality of buffers each connected to one of a plurality of execution units, the plurality of execution units each executing the instructions by accessing a memory and a global register (Note Fig. 1, elements 1, 3, 4, 6, 8-11 and 19 and the corresponding sections of the disclosure)
- a plurality of instruction sequences not executable in parallel because of data dependency ("Instruction N-2 is not issued in the instant cycle due to the data-dependence" in col. 11 line 67 to col. 12 line 1)
- non-speculative instructions is located before each instruction sequence including speculative instructions (Note col. 12 lines 10-50, wherein the execution of the instruction sequences is described. In step 6-1, non-speculative instruction, identified by the "0" identifier, is executed. In step 6-3, speculative instruction, identified by the "1" identifier, is executed.)
- the plurality of instruction sequences are aligned in correspondence with each of the plurality of buffers (Note Figure 1, items 2, 3 and 4 and the corresponding sections of the disclosure.)
- a task number representing the instruction sequence and a corresponding buffer is assigned to each instruction (Note Figure 1, items 2, 3 and 4 and the corresponding sections of the disclosure. Each instruction inherently has a task number in the system.)
- a condition instruction is replaced by a commit instruction, the commit instruction includes a condition task number to be accepted if the condition is not satisfied and task numbers to be rejected if the condition is satisfied ("Only when they satisfy all of these conditions, it forwards them to the instruction issuing circuit" in col. 10 lines 40-42. The system issues a commit instruction once the condition is met, whereas if the condition is not met, it will reject the instruction.)

- a task window number generator configured to assign a task window number to a plurality of instruction sequences (Note Fig. 6 and the corresponding section of the disclosure. A number generator must inherently be present such that the proceeding and succeeding instruction sequences are arranged in the correct order.)
- an assignment unit configured to assign each instruction of aligned instruction sequences to each of the plurality of buffers, by referring to the task number("The instruction fetch unit prefetches instructions from the memory...and selectively writes them into the instruction fetch buffers..." in col. 7 lines 10-13. The system would inherently refer to each instruction by the task number dictated by the system.)
- a register update unit configured to update data in a register number ("The execution order management buffer stores the results of the speculative execution accompanied with their register numbers and modes." in col. 7 lines 52-54)
- a memory update unit configured to update data in a memory address accessed by a particular instruction sequence ("a fetch controlling device for...incrementing its address every time an instruction is fetched from the memory..." in col. 3 lines 6-9)

substantially as claimed.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Kimura et al teach each instruction sequence including a flag representing possession of the register number of the global register as claimed ("The scoreboard includes 32 flags of 2-bit, one for each register in the register file" a 1-bit indicates the speculative execution, while the other 1-bit does the non-speculative execution" in col. 8 lines 41-44)

Regarding claim 3:

The rejection of claim 2 is incorporated, and further, Kimura et al teach the plurality of instruction sequences is aligned so that the number of aligned instructions is equal to the number of the plurality of execution units (Note at least Figure 1 and the corresponding sections of the disclosure. The system would inherently align only as many instructions are there are execution units, as the system could not execute more than that.)

Regarding claim 4:

The rejection of claim 3 is incorporated, and further, Kimura et al teach the instruction sequence speculatively executable is the instruction sequence to be executed if the condition is not satisfied and the instruction sequence to be executed if the condition is satisfied, and wherein the instruction sequence not speculatively executable is the instruction sequence including the commit instruction ("Only when they satisfy all of these conditions, it forwards them to the instruction issuing circuit" in col. 10 lines 40-42. The instructions are issued with a commit instruction.)

Regarding claim 5:

The rejection of claim 4 is incorporated, and further, Kimura et al teach a commit instruction representing a branch condition instruction as claimed ("three types of Branch with Condition Code Instructions..." in col. 6 lines 49-50)

Regarding claim 6:

The rejection of claim 3 is incorporated, and further, Kimura et al teach a loop condition instruction as claimed (Note Fig. 4 and the corresponding section of the disclosure.)

Regarding claim 7:

The rejection of claim 3 is incorporated, and further, Kimura et al teach a global register comprising a plurality of register numbers as claimed (Note Fig. 1, item 20 and the corresponding section of the disclosure, and further, col. 4 lines 5-11)

Regarding claim 8:

The rejection of claim 7 is incorporated, and further, Kimura et al teach an instruction decoder configured to decode a plurality of the instructions in order as claimed (Note Fig. 3 and the corresponding section of the disclosure.)

Regarding claim 9:

The rejection of claim 8 is incorporated, and further, Kimura et al teach an instruction decoder decoding the instruction including the flag, and setting the register number in the global register represented by the flag as claimed ("The scoreboard managing circuit checks which registers are in operation by referring to the scoreboard, and set the flags in the scoreboard based on the decoding of the decoders..." in col. 10 lines 19-22)

Regarding claim 10:

The rejection of claim 3 is incorporated, and further Kimura et al teach a plurality of queues, each of the plurality of queues exclusively storing the instructions by first in first out as claimed ("The

instruction fetch buffers...send the prefetched instructions to the instruction fetch buffer using FIFO(First-In-First-Out) memories." in col. 7 lines 25-27)

Regarding claim 11:

The rejection of claim 10 is incorporated, and further Kimura et al teach an assignment unit assigning each instruction of the aligned instruction sequences to the queue in the execution buffer corresponding to the task number of each instruction, comprising an operand condition decision unit which repeatedly selects one instruction from each instruction at a head position of each queue in the execution buffer by priority order, and indicates the execution buffer to transfer the one instruction to the execution unit connected to the execution buffer as claimed ("The instruction issuing circuit 39 includes four selectors 39a-39d, and it issues instructions forwarded from the instruction issue controlling circuit 40 to the executing units 8-11 in parallel after adding an identifier to each instruction: an identifier "1" for the speculative execution, and an identifier "0" for the non-speculative one" in col. 10 lines 27-32)

Regarding claim 12:

The rejection of claim 1 is incorporated, and further, Kimura et al teach incrementing the task window n umber by one when the commit instruction is detected as claimed (Note col. 2 line 66 to col. 3 line 17.)

Regarding claim 13:

The rejection of claim 9 is incorporated, and further, Kimura et al teach a plurality of local registers respectively connected to each of the plurality of execution units as claimed (Note Fig. 10, which

displays a list of Register numbers an instruction is written to, and the execution result of the instruction.)

Regarding claim 14:

The rejection of claim 13 is incorporated, and further, Kimura et al teach a register update unit updating data in the register number of the global register represented by the flag in the particular instruction sequence using the execution result as claimed ("outputs the execution results to the execution order management circuit, which writes them directly into the register file..." in col. 11 lines 42-44)

Regarding claim 15:

The rejection of claim 13 is incorporated, and further, Kimura et al teach a register update unit which does not update data in the register number of the global register as claimed (Note col. 10 lines 33-43. The instruction issuing circuit rejects instructions that do not meet the criteria, which in turn does not update the data in the register.)

Regarding claim 16:

The rejection of claim 1 is incorporated, and further, Kimura et al teach a memory update unit which temporarily preserves the execution result of a store instruction as claimed ("the execution result managing means includes temporary for storing means storing a set of the execution results of the executing units..." in col. 22 lines 58-61)

Regarding claim 17:

The rejection of claim 16 is incorporated, and further, Kimura et al teach a memory update unit which updates data in the address of the memory represented by the store instruction as claimed ("the temporary storing means stores register numbers of the execution results when the results are to be stored into registers, and stores memory addresses thereof when they are to be stored in the memory." in col. 22 lines 63-67)

Regarding claim 18:

The rejection of claim 16 is incorporated, and further, Kimura et al teach a memory update unit which does not update data in the address of the memory as claimed (Note that col. 22 lines 63-67 disclose storing into memory when the results only when the results are to be stored, consequently, the system will inherently not update data in the address of the memory when an instruction is not meant to be stored.)

Regarding claim 19:

The rejection of claim 16 is incorporated, and further, Kimura et al teach a load buffer which temporarily preserves a load instruction from memory as claimed (Note Fig. 1 elements 3 and 4 and the corresponding sections of the disclosure.)

Regarding claim 20:

The rejection of claim 19 is incorporated, and further, Kimura et al teach an execution unit which executes the load instruction in a particular instruction, and decides whether the load instruction depends on the execution result of the store instruction as claimed ("The processor may further

comprise a data-dependence detecting device for detecting data-dependence among a plurality of the decoded instructions by referring to a plurality of decoding results..." in col. 3 lines 45-48)

Regarding claim 21:

The rejection of claim 20 is incorporated, and further, Kimura et al teach a load buffer which loads the execution result of the store instruction as claimed ("Instruction N-2 is not issued until Instruction N-3 has been completed due to data-dependence." in col. 11, lines 35-37. Further, all instruction are stored in an instruction fetch buffer.)

Regarding claim 22:

The rejection of claim 21 is incorporated, and further, Kimura et al teach the load buffer loading data stored in the address of the memory as claimed ("The instruction issuance allowing device may identify instructions with issuable ones by confirming that the decoding results of the plurality of the decoding device have no data-dependence among each other from the detecting result of the data-dependence detecting device..." in col. 3 lines 61-65)

Regarding claim 23:

Claim 23 is directed to a method for generating a program to perform the actions as described in claim 1, and are rejected for the reasons set forth in connection with claim 1.

Regarding claim 24:

Claim 24 is directed to a computer readable memory containing computer readable instructions in a computer for performing the actions as described in claim 1, and are rejected for the reasons set forth in connection with claim 1.

Response to Arguments

7. Applicant's arguments filed 08 March 2004 have been fully considered but they are not persuasive.

The objections to the drawings, specification, and abstract as stated in the prior office action have been withdrawn.

Per claim 23:

The applicant states that Kimura et al does not disclose moving an instruction sequence speculatively executable forward of an instruction sequence not speculatively executable in the program. However, as stated above in regards to 35 U.S.C. § 112 1st paragraph, this is considered by the Examiner to constitute new matter which was not adequately described in the originally filed specification, and as such, the arguments that Kimura et al do not disclose moving an instruction sequence speculatively executable forward of an instruction sequence not speculatively executable in the program is considered moot. Further, the applicant merely alleges that Kimura et al does not disclose replacing a condition instruction by a commit instruction, the commit instruction including a condition, task numbers to be accepted if the condition is not satisfied and task numbers to be rejected if the condition is satisfied. However, as shown above, Kimura et al was shown to embody these elements. For these reasons, the rejection of claim 23 is considered proper and maintained.

Per claims 1 and 24:

The applicant states that claims 1 and 24 include similar recitations as claim 23, and as such, the rejections of claims 1 and 24 are considered proper and maintained for the reasons stated above in regards to claim 23.

Per claims 2-22:

The applicant states that claims 2-22 are allowable as being dependent on independent claim 1. However, as shown above, the rejection of independent claim 1 has been maintained, and as such, the argument that claims 2-22 are allowable as being dependent on an allowable base claim is considered moot.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (703)305-4627. The examiner can normally be reached on Monday - Friday, 9:00 am - 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trent J Roche
Examiner
Art Unit 2124

TJR

TODD INGBERG
PRIMARY EXAMINER